Course MICROELECTRONICS

Chapter: CMOS

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Source of figures:
Jaeger/Blalock: Microelectronic Circuit Design,
McGraw-Hill
Course Content

Introduction and Milestones in Microelectronics
Solid-state Electronics
Solid-state Diodes and Diode Circuits
Field-effect Transistors (FET)
Bipolar Junction Transistors (BJT)
Integrated Transistor circuits
Introduction to Digital Microelectronics
NMOS Logic Circuits
Complementary MOS Logic (CMOS)
Bipolar Logic Circuits
Semiconductor Memories
Application Specific Integrated Circuits (ASIC)
Microelectronic Technology
Chapter Content

The CMOS Inverter / CMOS Inverter

Dynamic Behavior / Dynamisches Verhalten

CMOS NOR and NAND Gates / CMOS NOR und NAND Gatter

Complex CMOS Logic Gates / Komplexe CMOS Gatter

CMOS Transmission Gate / CMOS Transmission Gate
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The **CMOS Inverter** / CMOS Inverter

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**CMOS Transmission Gate** / CMOS Transmission Gate
CMOS Technology

- Complementary MOS, or CMOS, needs both PMOS and NMOS devices for the logic gates to be realized.

- The concept of CMOS was introduced in 1963 by Wanlass and Sah, but it did not become common until the 1980’s as NMOS microprocessors were dissipating as much as 50 W and an alternative design technique/technology was needed.

- CMOS dominates digital IC design today.
MOTOROLA’s PowerPC 620 (32/64 Bit RISC)
CMOS Inverter

(a) Circuit schematic for a CMOS inverter
(b) Simplified operation model with a high input applied
(c) Simplified operation model with a low input applied
CMOS Inverter Technology

- The CMOS inverter consists of a PMOS device and an NMOS device, but they need to be fabricated on the same wafer.
- To accomplish this, the technique of “n-well” implantation is needed as shown in this cross-section of a CMOS inverter.
PMOS & NMOS Transistors Drain Currents

**NMOS** \( (v_{GS} \geq V_{TN}) \)

**Linear (Triode) Region**: \( i_D = K_n' \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \)

**Saturation Region**: \( i_D = \frac{K_n'}{2} \frac{W}{L} \left( v_{GS} - V_{TN} \right)^2 \left( 1 + \lambda v_{DS} \right) \)

**PMOS** \( (v_{GS} \leq V_{TP}) \)

**Linear (Triode) Region**: \( i_D = K_p' \frac{W}{L} \left( v_{GS} - V_{TP} - \frac{v_{DS}}{2} \right) v_{DS} \)

**Saturation Region**: \( i_D = \frac{K_p'}{2} \frac{W}{L} \left( v_{GS} - V_{TP} \right)^2 \left( 1 + \lambda v_{DS} \right) \)
Static Characteristics of the CMOS Inverter

- The figure shows the two static states of operation with the circuit and simplified models.

- Notice that \( V_H = 5V \) and \( V_L = 0V \), and that \( I_D = 0A \) which means that there is no static power dissipation.
CMOS Voltage Transfer Characteristics (1)

- The VTC shown is for a CMOS inverter that is symmetrical ($K_p = K_n$)

- Region 1: $v_O = V_H$
  $v_I < V_{TN}$

- Region 2: $|v_{DS}| \geq |v_{GS} - V_{TP}|$

- Region 4: $v_{DS} \geq v_{GS} - V_{TN}$

- Region 5: $v_O = V_L$
  $v_I > V_{DD} - |V_{TP}|$
CMOS Voltage Transfer Characteristics (2)

- The simulation results show the varying VTC of the inverter as $V_{DD}$ is changed.

- The minimum voltage supply for CMOS technology is $V_{DD} = 2V_T \ln(2)$ V.
Noise Margins for the CMOS Inverter
CMOS Inverter Layout

- Two methods of laying out a CMOS inverter are shown
- The PMOS transistors lie within the n-well, whereas the NMOS transistors lie in the p-substrate
- Polysilicon is used to form common gate connections, and metal is used to tie the two drains together
CMOS Inverter Layout

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Propagation Delay Estimate (1)
Propagation Delay Estimate (2)

\[
\tau_{PHL} = R_{onN} C \left\{ \ln \left[ 4 \left( \frac{V_H - V_{TN}}{V_H + V_L} \right) - 1 \right] + \frac{2V_{TN}}{V_H - V_{TN}} \right\}
\]

\[
R_{onN} = \frac{1}{K_n (V_H - V_{TN})}
\]

\[
\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \tau_{PHL}
\]

- If it is assumed the inverter is “symmetrical” with 
  \((W/L)_P = 2.5(W/L)_N\), then \(\tau_{PLH} = \tau_{PHL}\)
Rise and Fall Times

- The rise and fall times are given by the following approximate expressions:

\[ t_f = 2\tau_{PHL} \]
\[ t_r = 2\tau_{PLH} \]

Symmetrical inverter:

\[ t_f = t_r \]
Static Power Dissipation

- CMOS logic is considered to have no static power dissipation

- This is not completely accurate since MOS transistors have leakage currents associated with the reverse-biased drain-to-substrate connections as well as sub-threshold leakage current between the drain and source
Dynamic Power Dissipation

- There are two components that add to dynamic power dissipation:

1) **Capacitive load charging** at a frequency $f$ given by: $P_D = CV^2_{DD}f$

2) The **current** that occurs during **switching** which can be seen in the figure
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CMOS NOR Gate

\[ Y = \overline{A + B} \]
CMOS NOR Gate Layout
CMOS NOR Gate

\[ Y = \overline{A + B + C} \]

It is possible to extend this same design technique to create multiple input NOR gates.
CMOS NAND Gate

\[ Y = \overline{A \cdot B} \]
Multi-Input CMOS NAND Gates

\[ Y = A \cdot B \cdot C \cdot D \cdot E \]
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Complex CMOS Logic Gate Design

Diagram of a CMOS logic gate with PMOS and NMOS switching networks.
Complex CMOS Logic Gate Example

\[ Y = \overline{A + B} \cdot (C + D) \]
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CMOS Transmission Gate

- The CMOS transmission gate (T-gate) is a useful circuits for both analog and digital applications.

- It acts as a switch that can operate up to $V_{DD}$ and down to $V_{SS}$. 
CMOS Transmission Gate (2)

- The main consideration that needs to be considered is the equivalent on-resistance which is given by the following expression:

\[ R_{EQ} = \frac{R_{onp} R_{onn}}{R_{onp} + R_{onn}} \]
Summary

- In CMOS logic each gate contains both an NMOS and a PMOS switching network and every logical input is connected to at least one NMOS and one PMOS transistor.
- The high and low output voltage are $V_{DD}$ and $V_{SS}$ and therefore the noise margins are maximal.
- NAND gates, NOR gates and complex CMOS logic gates can all be designed as for NMOS circuitry. The NMOS and the PMOS switching networks are behavioral or structural dual.
- CMOS power dissipation is determined by the energy required to charge and discharge the load capacitance at the desired switching frequency. The static power dissipation is nearly disappearing.
- During switching of the CMOS gate a pulse of current occurs between the positive and negative power supplies. This current causes an additional component of the power dissipation in CMOS gates that can be as much as 20 to 30 percent of the dissipation resulting from charging and discharging the load capacitance.
- A new bidirectional circuit element, the CMOS transmission gate that utilizes the parallel connection of an NMOS and a PMOS transistor was introduced. When the transmission gate is on, it provides a low-resistance connection between its input and output terminals over the entire input voltage range.